Method and Apparatus for Driving STN LCD

Inventors: Tae-Kwang Park and Keunmyung Lee

RELATED APPLICATION

This application claims the benefit of co-pending U.S. Provisional Application Ser. No. 60/271452, filed February 27, 2001, entitled "Method and Apparatus for Driving STN LCD."

BACKGROUND OF THE INVENTION

Technical Field

This invention in general relates to semiconductor circuits. More specifically, this invention relates to circuits for driving STN liquid crystal displays.

Description of the Related Art

FIG. 1 shows a structure of conventional supertwisted nematic ("STN") liquid crystal display ("LCD") module, which comprises an LCD panel 101 consisting of row electrodes 102 and column electrodes 103, a row driver 104 for applying row driving voltages to the row electrodes 102, and a column driver 105 for applying column driving voltages to the column electrodes 103. Pixels are formed at every cross-section of the row and column electrodes, such as at 106. Each pixel changes to black, white, or a different shade of gray or color depending on the voltages applied by the corresponding row and column electrodes across the liquid crystal to change the light transmittance.

In order to display a frame of data, voltages must be applied to all the individual

electrodes so that all the pixels are addressed. In conventional sequential driving methods, each row electrode is selected sequentially (also called "scanning electrode") and the pixel data values corresponding to the selected scanning electrode are applied to the corresponding column electrode. Each frame needs to be displayed repeatedly to maintain a certain RMS value of each pixel so that the frames can be recognized by human eyes without any flickering.

In the cases where the display data needs to be changed very fast such as in displaying moving pictures, the conventional sequential driving methods suffers so-called a "frame response phenomenon." In order to drive a high-speed or large-panel liquid crystal, driving pulses of high-amplitude and short pulse width are required, which causes uneven brightness of the LCD panel.

Multi-line addressing (MLA) methods have been suggested for driving flat panel devices as alternatives to sequential driving methods. According to the MLA methods, multiple row electrodes are selected simultaneously to enable multiple selection of row electrodes within a frame cycle to increase the effective duty cycle of the row voltage application. Typically, orthogonal signals are applied to a set of row electrodes so that the individual electrodes can maintain the same effective RMS values within a frame.

When orthogonal row signals are simultaneously applied to a set of row electrodes, new column signals must be determined to maintain the correct pixel data. In other words the voltage levels to column electrodes should be recalculated, taking into account of simultaneous driving of multiple row electrodes.

FIG. 2 shows a block diagram of a conventional 4-line MLA column driver. A display data RAM 121 stores data for display and outputs some of the display data for latch by a display data latch 122. In order to facilitate recalculation of the column

signals, orthogonal row signals Fi(t) applied to a set of row electrodes are compared with the display data of the same set of row electrodes at an XOR block 123 column by column to find mismatches between the orthogonal signals Fi(t) and display data for each column. A decoder block 124 calculates mismatch numbers based on the result of mismatches from the XOR block 123. After the mismatch numbers are latched at an output latch block 125, the data levels of the mismatch numbers are shifted at a level shifter block 126, and a voltage selector 127 selects a voltage level among 5 different voltages levels based on the level-shifted mismatch numbers.

Because the conventional MLA driver uses data and output latches, it requires a large chip area in its implementation, which adversely affect the performance of the driver. Therefore, there is a need for a new driver that requires less number of circuit components and chip area to improve the performance.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an efficient LCD driver optimized in the chip area to improve the performance.

The foregoing and other objects are accomplished by a virtual-line MLA using multiple-output display data RAM. A preferred embodiment comprises a 3-line output display data for storing display data, an XOR block for finding mismatches between each 3-line output set of the stored display and orthogonal function signals, a decoder block for calculating mismatch numbers, a level shifter block for shifting the data level of the mismatch numbers to another level, and a voltage selector block for selecting a voltage level from 2 levels of voltage. Because data latches and output latches are not necessary, the driver of the present invention achieves a significant reduction in the

circuit components and chip size without compromising the display quality.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a conventional LCD.

Figure 2 is a block diagram of a conventional MLA driver.

Figure 3 is a block diagram of a new MLA driver of the present invention.

Figure 4 is an illustration of an embodiment of a display data RAM according to the present invention.

Figure 5 is an illustration of an alternative embodiment of a display data RAM. According to the present invention

Figure 6 is a schematic block diagram of the MLA driver.

Figure 7 is an illustration of an example of orthogonal functions used for the virtual-line MLA of the present invention.

Figure 8 is a timing diagram for the MLA driver according to the present invention.

Figure 9 is an illustration of a structure of a display data RAM for color display in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 3 shows a block diagram of a preferred embodiment of an MLA driver of the present invention. The preferred embodiment includes a 3-line output display data RAM 201 that is capable of simultaneously/concurrently outputting 3 lines of data. Because 3-line data items are outputted simultaneously, display data latches are no longer needed for calculating mismatch numbers with orthogonal functions. Moreover,

since the output data items from the 3-line output display data RAM are synchronized to the system clock, the output latches are also unnecessary. In the preferred embodiment, the display data RAM 201 stores 168 rows and 128 columns of bits that represents pixel data for a 168x128 display.

The present invention employs a virtual-line MLA, where a "virtual" row signal is additionally provided after every three "real" row signals. The virtual row signal is not used in accessing stored data. Instead, the virtual row signal is used only for the purpose of simplifying calculation of mismatch numbers and thereby facilitating calculation of column signals. Three real row signals and one virtual row signal constitute a set of 4-line orthogonal signals that combine with display data to produce column signals that would produce the correct display when multiple row electrodes are simultaneously driven.

The following table compares the method of calculating mismatch numbers using the orthogonal function of the present invention with the convention method. By employing 3 real lines and a virtual line, only 2 kinds of mismatch numbers may be used, namely, "1" and "3", compared to the conventional 4-line MLA using 5 kinds of mismatch numbers of "0", "1", "2", "3", "4".

Mismatch Number	Mismatch Number	Comment
Conventional art	Present Invention	
0 (-Vx2)	1 (-Vx1)	Add one mismatch
1 (-Vx1)	1 (-Vx1)	Not converted
2 (Vc)	3 (+Vx1)	Add one mismatch
3 (+Vx1)	3 (+Vx1)	Not converted
4 (+Vx2)	-	Not happen

FIG. 4 schematically shows an embodiment of the 3-line output display data RAM. As the display is partitioned into scan blocks of 3 scan lines, the display data RAM is also partitioned into blocks, such as block 0, 221, each block consisting of 3 rows. Scanning is performed on blocks of rows rather than individual rows.

For column 0, the first line outputs at each scan I(0,0), I(3,0), I(6,0), ... I(3x(block number), 0). The second line outputs at each scan I(1,0), I(4,0), I(5,0), ... I(3x(block number)+1, 0) The third line outputs at each scan I(2,0), I(5,0), I(6,0), ..., I(3x(block number)+2, 0). At the first scan, for example, the three lines output I(0,0), I(1,0), and I(2,0) simultaneously, which are combined with orthogonal function signals.

Similarly, for column 1, the first line outputs at each scan: I(0,1), I(3,1), I(6,1), ... I(3x(block number), 1). The second line outputs at each scan: I(1,1), I(4,1), I(5,1), ... I(3x(block number)+1, 1) The third line outputs at each scan: I(2,1), I(5,1), I(6,1), ..., I(3x(block number)+2, 1). At the first scan, for example, the three lines output I(0,1), I(1,1), and I(2,1) simultaneously, which are combined with orthogonal function signals.

FIG. 5 shows an alternative embodiment of a display data RAM of the present invention. The display is partitioned into scan blocks of 3 scan lines. The display data RAM is also partitioned, but the 3 display data items in adjacent rows along the same column are arranged within the display data RAM in a horizontal fashion to achieve a more efficient layout. For example, I(0,0), I(1,0), and I(2,0) are arranged in horizontally rather than vertically.

FIG. 6 schematically illustrates the blocks of FIG. 3 in more detail except the display data RAM. The XOR block 202 consists of triples of XOR gates, such as 261. The three rows of display data along the same column currently output by the display RAM 201, such as I(0,0), I(1,0), I(2,0), are compared with orthogonal row signals $F_i(t)$

at the XOR block 202 to compute mismatch numbers. The decoder block 203 consists of 128 individual decoders, such as 262, each having 3 inputs for generating the number of mismatches for each column. The mismatch numbers are used by the level shifter block 204 having 128 1-bit level shifters, such as 263, and the voltage selector 205 having 128 individual voltage selectors, such as 264, each selecting either +Vx1 or –Vx1.

Each individual voltage selector 264 selects +Vx1 for a mismatch number of "1" and –Vx1 for a mismatch number of "3". Since a voltage level is selected from 2 voltage levels, the construction is simpler than that of the conventional method of selecting one voltage level from 5 voltage levels of –Vx2, -Vx1, Vc, +Vx1, and +Vx2.

As mentioned above, there is no need for display data latches and output data latches that were essential in the implementation of the conventional MLA methods. With the use of the multi-line output type RAM of the present invention, the circuit components of a column driver are reduced, resulting a smaller chip size.

FIG. 7 shows an example of orthogonal functions of signals applied to scan lines. The scan lines are divided into blocks where each block is made of block of 3 lines and 1 virtual line rather than a block of 4 lines in the convention MLA. There are 32 scan lines in total, which are 24 lines actually used and 8 virtual lines.

FIG. 8 shows a timing diagram of the MLA method of the present invention. The frame start signal 302 is first generated in sync with the system clock 301. The scan block signal 303 counts the address of display data RAM blocks. At the rising edge of the system clock display, the display data of each block are outputted as a display data signal 304 and, at the same time, the signal for the mismatch numbers 306 are generated based on the display data signal 304 and row orthogonal signals 305.

FIG. 9 shows a block diagram of another display data RAM for use with a color display in accordance with the present invention. The example shows a RAM 321 consisting of 56 rows by 128 x 3 columns of addressable bits for storing RGB pixel data. Each primary color of RGB is represented by 3 bits making 8 different shades available for each primary color, and thus 512 different colors in combinations. Each bit is stored in a memory cell such as 322.

When a scan block, such as scan block 325, is activated, three bits for Red in the first row, such as 322, 323 and 324, are combined to select a gray level Red by making use of a multiplexer, such as 326, which selects one gray level as an output, such as R(0,0) 327 out of 8 predetermined gray levels, Gray0 through Gray7. Three bits for Red in the second row within the activated scan block 325 are combined by a multiplexer to produce a gray-level output R(1,0). Similarly, three bits for Red in the third row within the activated scan block are combined by a multiplexer to produce a gray-level output R(2,0). Each three gray level colors in the adjacent rows along the same column, such as R(0,0), R(1,0), and R(2,0), are then combined with the orthogonal functions to calculate the mismatch numbers.

While the invention has been described with reference to preferred embodiments, it is not intended to be limited to those embodiments. It will be appreciated by those of ordinary skilled in the art that many modifications can be made to the structure and form of the described embodiments without departing from the spirit and scope of this invention.